CLASS XII – PHYSICS (042)
STEP-BY-STEP SOLUTIONS AND MARKING SCHEME

Chapter 14: Semiconductor Electronics – Practice Paper (35 Marks)

Answer key – Section A

Q.	1	2	3	4	5	6	7	8	9
Ans.	(c)	(a)	(d)	(b)	(c)	(a)	(d)	(a)	(c)

Marks are shown in square brackets. Equivalent correct methods are acceptable. Key relations: $n_e n_h = n_i^2$; barrier = $V_0 - V$ (forward), $V_0 + V$ (reverse); $r_d = \Delta V/\Delta I$; ripple frequency = f (half-wave), 2f (full-wave); time constant $\tau = R_L C$.

SECTION A

Q.1 (c)

In X the valence and conduction bands overlap ($E_g \approx 0$), so it is a metal. Y has E_g = 1.1 eV (< 3 eV), so it is a semiconductor. Z has E_g = 5.4 eV (> 3 eV), so it is an insulator. **[1]**

Q.2 (a)

A level just above E_V (0.05 eV) is an acceptor level. It is produced by a trivalent dopant (B, Al, In). Electrons from the valence band jump to it easily, leaving holes, so the crystal is p-type with holes as majority carriers. **[1]**

Q.3 (d)

D_1 is forward biased (ideal: zero resistance), so its branch carries I = 10 V/2 kΩ = 5 mA. D_2 is reverse biased (ideal: infinite resistance), so its branch carries no current. Total current = 5 mA. **[1]**

Q.4 (b)

From the graph, the period T = 10 ms, so the input frequency f = 1/T = 100 Hz. A full-wave rectifier gives two pulses per input cycle, so the output frequency = 2 × 100 = 200 Hz. **[1]**

Q.5 (c)

The cut-in voltage of curve 1 is about 0.2 V, that of germanium. The cut-in voltage of curve 2 is about 0.7 V, that of silicon. **[1]**

Q.6 (a)

Forward bias lowers the barrier to $V_0 - V$ = 0.4 V (curve Z). Reverse bias raises it to $V_0 + V$ = 1.0 V (curve X). The no-bias barrier is 0.7 V (curve Y). So X, Y, Z are reverse, no bias, forward. **[1]**

Q.7 (d)

X has valency 3, so it makes only three bonds with its four neighbours and leaves a vacancy (hole). It accepts an electron, so it is an acceptor and the crystal is p-type. **[1]**

Q.8 (a)

Both statements are true. Under forward bias the lowered barrier lets many majority carriers cross (mA), while under reverse bias only the few minority carriers are swept across (μA). R correctly explains A. **[1]**

Q.9 (c)

A is true: at 0 K there are no free electrons in the conduction band, so the pure semiconductor behaves like an insulator. R is false: at 0 K the conduction band is completely empty (the valence band is full). **[1]**

SECTION B

Q.10

(a) At P the applied voltage (0.3 V) is less than the cut-in voltage of silicon (about 0.7 V). The barrier is lowered only slightly, so very few carriers have enough energy to cross it, and the current is almost zero. **[1]**

(b) The reverse current is due to minority carriers, which are swept across the junction by the barrier field. Their number depends on thermal generation, not on the applied voltage, so the current is almost constant (reverse saturation current) until breakdown. **[1]**

Q.11

(a) The crystal is n-type (the donor atom, with 5 valence electrons, gives a free electron). An example of the dopant is arsenic (or phosphorus, antimony). **[1]**

(b) $n_e \approx N_D = 2 \times 10^{22}\ m^{-3}$. From $n_e n_h = n_i^2$: $n_h = (2 \times 10^{16})^2/(2 \times 10^{22}) = 4 \times 10^{32}/2 \times 10^{22} = 2 \times 10^{10}\ m^{-3}$. **[1]**

Q.12

(A) (a) The diode is forward biased and drops 0.7 V. The voltage across R = 3.7 − 0.7 = 3.0 V. I = 3.0/100 = 0.03 A = 30 mA. **[1]**

(b) $P = I^2R = (0.03)^2 \times 100 = 0.09$ W (or $P = 3.0 \times 0.03 = 0.09$ W). **[1]**

OR (B) (i) The p-side is at −3 V and the n-side at −9 V. The p-side is at the higher potential, so the diode is forward biased. **[1]**

(ii) The p-side is at +6 V and the n-side at +10 V. The p-side is at the lower potential, so the diode is reverse biased. **[1]**

Q.13

(a) When A is positive with respect to the centre tap, the p-side of D_1 is positive, so D_1 conducts (D_2 is reverse biased). The current in R_L flows from X to Y. **[1]**

(b) A capacitor (capacitor filter) is connected across R_L. It charges up to the peak voltage and discharges only slowly through R_L between the pulses, which reduces the ripple and gives a nearly steady dc output. **[1]**

SECTION C

Q.14

(a) Holes diffuse from p to n and electrons diffuse from n to p because of the concentration gradient. Each electron that leaves the n-side leaves behind an immobile positive donor ion; each hole that leaves the p-side leaves behind an immobile negative acceptor ion. So the n-side of the depletion region is positively charged and the p-side negatively charged. **[1]**

(b) Forward bias: $V_0 - V = 0.7 - 0.3 = 0.4$ V. Reverse bias: $V_0 + V = 0.7 + 0.3 = 1.0$ V. **[1]**

(c) The diffusion current (p to n) and the drift current (n to p) are equal in magnitude and opposite in direction, so the net current is zero. **[1]**

Q.15

(A) (a) $r_f = \Delta V/\Delta I = (0.76 - 0.70)\ V/(40 - 10)\ mA = 0.06/0.030 = 2\ \Omega$. **[1]**

(b) $r_r = V/I = 10\ V/2\ \mu A = 10/(2 \times 10^{-6}) = 5 \times 10^6\ \Omega$. **[1]**

(c) $r_r/r_f = 5 \times 10^6/2 = 2.5 \times 10^6$. The diode offers a very low resistance in forward bias and a very high resistance in reverse bias, so it conducts in one direction only and can be used as a rectifier. **[1]**

OR (B) (a) P has a donor level E_D just below the conduction band, so P is n-type (majority carriers: electrons). Q has an acceptor level E_A just above the valence band, so Q is p-type (majority carriers: holes). **[1]**

(b) The impurity level is only about 0.05 eV from the conduction band (or valence band), so thermal energy at room temperature is enough to ionise nearly all the impurity atoms. The band gap is 1.1 eV, which is far larger than the thermal energy, so only a very few electrons cross it. **[1]**

(c) $n_h = n_i^2/n_e = (2 \times 10^{16})^2/(4 \times 10^{21}) = 4 \times 10^{32}/4 \times 10^{21} = 10^{11}\ m^{-3}$. **[1]**

Q.16

(a) The capacitor charges to the peak voltage while the rectified voltage rises. When the voltage falls, the capacitor discharges slowly through R_L and supplies the load, so the output does not fall to zero between pulses and the ripple is reduced. **[1]**

(b) $\tau = R_L C = 10^4\ \Omega \times 100 \times 10^{-6}\ F = 10^4 \times 10^{-4} = 1$ s. **[1]**

(c) For a full-wave rectifier the pulse frequency is $2 \times 50 = 100$ Hz, so the time between pulses is $1/100 = 0.01$ s $= 10$ ms. $\tau = 1$ s is 100 times larger than this, so the capacitor loses very little charge between pulses. The output stays almost constant, close to the peak voltage. **[1]**

SECTION D

Q.17

(i) (c). In forward bias the majority carriers cross the lowered barrier (mA). In reverse bias the barrier is raised and only the minority carriers drift across (μA). **[1]**

(ii) (a). The forward current starts rising at about 0.7 V, the cut-in voltage of a silicon diode. **[1]**

(iii) (c). Increasing the reverse bias raises the barrier and widens the depletion region. The current, due to minority carriers, stays almost constant. **[1]**

(iv) (b). Voltage across the resistor $= 2.7 - 0.7 = 2.0$ V, so $I = 2.0/200 = 0.01$ A $= 10$ mA. **[1]**

OR (iv) (a). $R = V/I = 20\ V/(4 \times 10^{-6}\ A) = 5 \times 10^6\ \Omega$. **[1]**

SECTION E

Q.18

(A) (a) *Circuit (1):* The secondary of a transformer is connected in series with a p-n diode D and a load R_L; the output is taken across R_L. (A neat labelled diagram is required.) **[1]**

Working (1): During the positive half cycle of the input the p-side of the diode is positive, so it is forward biased and conducts, giving a voltage across R_L. During the negative half cycle it is reverse biased and there is no current in R_L. **[1]**

Waveforms (1): The input is a sine wave. The output consists of positive half-cycles only, with zeros during the negative half-cycles (unidirectional pulses, one per input cycle). **[1]**

(b) Peak current $I_0 = V_0/R_L = 10/500 = 0.02$ A $= 20$ mA. **[1]**

Half-wave output frequency = input frequency = 50 Hz. **[1]**

OR (B) (a) *Circuit (1):* The ends A and B of the secondary of a centre-tap transformer are connected to the p-sides of D_1 and D_2. Their n-sides are joined together, and the load R_L is connected between this junction and the centre tap. (A neat labelled diagram is required.) **[1]**

Working (1): When A is positive with respect to the centre tap, B is negative: D_1 conducts and D_2 does not. In the next half cycle B is positive and A is negative: D_2 conducts and D_1 does not. The current in R_L is in the same direction in both half cycles. **[1]**

Waveforms (1): The input at A and at B are sine waves in opposite phase. The output across R_L consists of positive pulses in both half-cycles (two pulses per input cycle). **[1]**

(b) Peak current $I_0 = 12/400 = 0.03$ A $= 30$ mA (each diode uses one half of the secondary). **[1]**

Full-wave output frequency $= 2 \times 50 = 100$ Hz. **[1]**

— End of Solutions —